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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,006	08/27/2001	David E. Kimble	TI-33210	7032

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EXAMINER	
SHERKAT, AREZOO	

ART UNIT	PAPER NUMBER
2131	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,006	KIMBLE ET AL.	
	Examiner	Art Unit	
	Arezoo Sherkat	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

This office action is responsive to Applicants amendment received on January 28, 2005. Figures 1a, 1b, 2a, and 2b have been amended. Claims 1-17 are pending as originally presented.

Response to Arguments

Applicant's arguments, see Remarks, pages 4-5, filed on January 28, 2005, with respect to the rejection(s)of claim(s) 1-17 under 35 U.S.C 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art reference as follows:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Buer, (U.S. Patent No. 6,148,365).

Regarding claims 1, 5, 7, and 9, Buer discloses a cryptographic system comprising:

a first FIFO data storage device having a primary write address to receive unprocessed data via a first data path into the first FIFO data storage device, a primary read address, a secondary read address and a secondary write address, and an encryption/decryption circuit configured to read the unprocessed data via the secondary read address, selectively encrypt or decrypt the unprocessed data read via the secondary read address to generate processed data, and write the processed data back into the first FIFO data storage device via the secondary write address, such that the processed data written back into the first FIFO data storage device can be read from the first FIFO data storage device via the primary read address (Col. 1, lines 65-67 and Col. 2-3, lines 1-67).

Regarding claims 2, 4, 8, 10, and 12, Buer discloses wherein the FIFO data storage device is a single port random access memory (Col. 2, lines 31-44).

Regarding claims 3, 6 and 11, Buer discloses further comprising:

a second FIFO data storage device having a primary write address to receive unprocessed data via a second data path into the second FIFO data storage device, a primary read address, a secondary read address and a secondary write address, and a switching circuit configured to multiplex between the first and second FIFO data storage devices such that the encryption/decryption circuit can parallel process the unprocessed data stored in the first and second FIFO data storage devices to generate respective processed data, and write the respective processed data back into the first and second

FIFO data storage devices via their respective secondary write addresses, such that the respective processed data written back into the first and second FIFO data storage devices can be read from the first and second FIFO data storage devices via their respective primary read addresses (i.e., note that it is known in the art to use multiple storage devices in parallel for load balancing, fast processing, and/or ... purposes)(Col. 1, lines 65-67 and Col. 2-3, lines 1-67).

Regarding claims 13 and 15, Buer discloses a method of performing data cryptography comprising the steps of:

providing a first FIFO memory having a primary write address, a secondary read address, a primary read address, and a secondary write address, writing data into the first FIFO memory via its primary write address, providing a second FIFO memory having a primary write address, a secondary read address, a primary read address, and a secondary write address, writing data into the second FIFO memory via its primary write address, providing a switcher configured to multiplex between the first and second FIFO memory secondary read addresses and the first and second FIFO memory secondary write addresses, multiplexing between the first and second FIFO memory secondary read addresses to selectively access the data written into the first and second FIFO memories (i.e., note that it is known in the art to use multiple storage devices in parallel for load balancing, fast processing, and/or ... purposes), selectively encrypting or decrypting the multiplexed data to generate processed data, writing processed data generated from data stored in the first FIFO memory back into the first

FIFO memory via its secondary write address, and writing processed data generated from data stored in the second FIFO memory back into the second FIFO memory via its secondary write address (Col. 1, lines 65-67 and Col. 2-3, lines 1-67).

Regarding claims 14 and 16-17, Buer discloses further comprising the step of reading the written processed data via the primary read address (Col. 3, lines 39-67 and Col. 4, lines 1-23).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kalkunte, (U.S. Patent No. 5,859,980),

Wang et al., (U.S. Patent No. 6,327,625),

YLONEN et al., (U.S. Publication No. 2002/0062344), and

Lubarsky et al., (U.S. Patent No. 5,062,104).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arezoo Sherkat whose telephone number is (703) 305-8749/(703) 272-3796. The examiner can normally be reached on 8:00-4:30 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (703) 305-9648/(703) 272-3796. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arezoo Sherkat
Patent Examiner
Group 2131
May 2, 2005

GUY LAMARRE
PRIMARY EXAMINER